What is claim d is:

1. A s miconductor memory device, comprising:

a cell array including bit lines arranged at a uniform pitch; and

a plurality of bit line selection transistors connected to respective bit line ends for selectively connecting said bit line to a sense amp, wherein said bit line selection transistors are translationally arrayed in a direction perpendicular to said bit line at an average array pitch greater than eight times said pitch of said bit lines.

2. The semiconductor memory device according to claim 1, wherein said average array pitch is related to an integer other than said bit line pitch multiplied by a power of 2.

3. The semiconductor memory device according to claim 1, wherein said bit line selection transistors are arrayed in said direction perpendicular to said bit line at two or more different array pitches.

4. The semiconductor memory device according to claim 1, wherein said bit line selection transistors are arrayed on a plurality of stages in the longitudinal direction of said bit line, having two or more different array stages corresponding to positions of said bit lines.

5. The semiconductor memory device according to claim 1, wherein said bit line selection transistors are laid out to have a gate width direction orthogonal to said bit line.

6. The semiconductor memory device according to claim 1, wherein said bit line selection transistors are laid out to have a gate length direction orthogonal to said bit line.

7. The semiconductor memory device according to claim 1, wherein a bit line selection transistor for selecting an even bit line and a bit line selection transistor for selecting an odd bit line adjacent thereto are formed to share a common source/drain diffusion layer, said common source/drain diffusion layer being connected to a sensing bit line that leads to a sense amp shared by said even bit line and said adjacent odd bit line.

8. The semiconductor memory device according to claim 1, wherein said cell array includes electrically erasable programmable non-volatile semiconductor memory cells arrayed.

9. The semiconductor memory device according to claim 8, wherein said non-volatile semiconductor memory

cells configure a NAND cell unit including a plurality of serially connected cells, each pair of adjacent cells sharing a source/drain diffusion layer.

10. An electronic card including said semiconductor memory device according to claim 9 mounted thereon.

11. An electronic device, comprising:

a card interface;

a card slot connected to said card interface; and

said electronic card according to claim 10 electrically connectable to said card slot.

12. The electronic device according to claim 11, wherein said electronic device comprises a digital camera.

13. A semiconductor memory device, comprising:

a cell array including bit lines arranged at a uniform pitch; and

a plurality of bit line selection transistors connected to respective bit line ends for selectively connecting said bit line to a sense amp, wherein said bit line selection transistors are translationally arrayed in a direction perpendicular to said bit line at an average array pitch deviated from an integer multiple of said pitch of said bit lines.

14. The semiconductor memory device according to claim 13, wherein said bit line selection transistors are arrayed in said direction perpendicular to said bit line at two or more different array pitches.

15. The semiconductor memory device according to claim 13, wherein said bit line selection transistors are arrayed on a plurality of stages in the longitudinal direction of said bit line, having two or more different array stages corresponding to positions of said bit lines.

16. The semiconductor memory device according to claim 13, wherein said bit line selection transistors are laid out to have a gate width direction orthogonal to said bit line.

17. The semiconductor memory device according to claim 13, wherein said bit line selection transistors are laid out to have a gate length direction orthogonal to said bit line.

18. The semiconductor memory device according to claim 13, wherein a bit line selection transistor for selecting an even bit line and a bit line selection transistor for selecting an odd bit line adjacent thereto are formed to share a common source/drain diffusion layer, said common source/drain diffusion layer being connected to

a sensing bit line that leads to a sense amp shared by said even bit line and said adjacent odd bit line.

19. The semiconductor memory device according to claim 13, wherein said cell array includes electrically erasable programmable non-volatile semiconductor memory cells arrayed.

20. The semiconductor memory device according to claim 19, wherein said non-volatile semiconductor memory cells configure a NAND cell unit including a plurality of serially connected cells, each pair of adjacent cells sharing a source/drain diffusion layer.

21. An electronic card including said semiconductor memory device according to claim 20 mounted thereon.

22. An electronic device, comprising:

a card interface;

a card slot connected to said card interface; and

said electronic card according to claim 21 electrically connectable to said card slot.

23. The electronic device according to claim 22, wherein said electronic device comprises a digital camera.